IN THE SPECIFICATION

Please rewrite the title as follows:

–ENCODING APPARATUS AND DECODING APPARATUS--.

Please insert the following new paragraphs at page 4, between lines 6 and 7:

--As another preferred embodiment, the invention discloses an encoding apparatus comprising: (a) a first encoding unit adapted to encode inputted data; (b) an interleaving unit adapted to interleave the inputted data; and (c) a second encoding unit adapted to encode an output of the interleaving unit. The encoding apparatus executes a first encoding algorithm using the first encoding unit, and executes a second encoding algorithm using the first encoding unit, the interleaving unit and the second encoding unit. The encoding apparatus shares the first encoding unit when the encoding apparatus executes the first and second encoding algorithms in parallel.

As another preferred embodiment, the invention discloses a decoding apparatus, comprising: (a) a first decoding unit adapted to decode inputted data; (b) a first interleaving unit adapted to interleave an output of the first decoding unit; (c) a second decoding unit adapted to decode an output of the first interleaving unit; and (d) a second interleaving unit adapted to interleave an output of the second decoding unit. The decoding apparatus executes a first decoding algorithm using the first decoding unit, and executes a second decoding algorithm using the first and second decoding units and the

first and second interleaving units. The decoding apparatus shares the first decoding unit when the decoding apparatus executes the first and second decoding algorithms in parallel.--

Please amend the Abstract as follows. A clean version of the amended Abstract is presented at page 5.

--An encoding apparatus includes a first encoding unit adapted to encode inputted data, an interleaving unit adapted to interleave the inputted data, and a second encoding unit adapted to encode an output of the interleaving unit. The encoding apparatus executes a first encoding algorithm using the first encoding unit, and executes a second encoding algorithm using the first encoding unit, the interleaving unit and the second encoding unit. Furthermore, the encoding apparatus shares the first encoding unit when the encoding apparatus executes the first and second encoding algorithms in parallel. ~~A partial circuit of an encoding circuit for realizing a first error correction encoding algorithm and a partial circuit of an encoding circuit for realizing a second error correction encoding algorithm are shared to realize these two algorithms by one error correction encoding circuit. A partial circuit of a decoding circuit for realizing a first error correction decoding algorithm and a partial circuit of a decoding circuit for realizing a second error correction decoding algorithm are shared to realize these two algorithms by one error correction encoding algorithms can therefore be realized by a simple and inexpensive circuit. A~~

~~plurality of error correction decoding algorithms can therefore be realized by a simple and inexpensive circuit.~~--